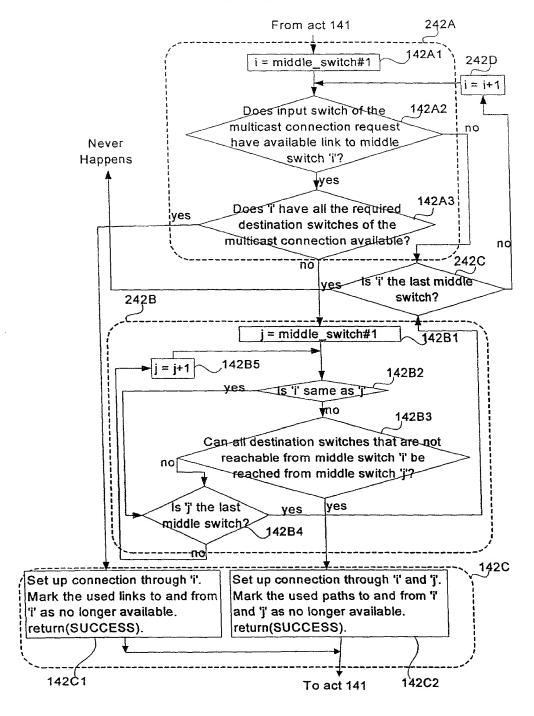
FIG. 4B





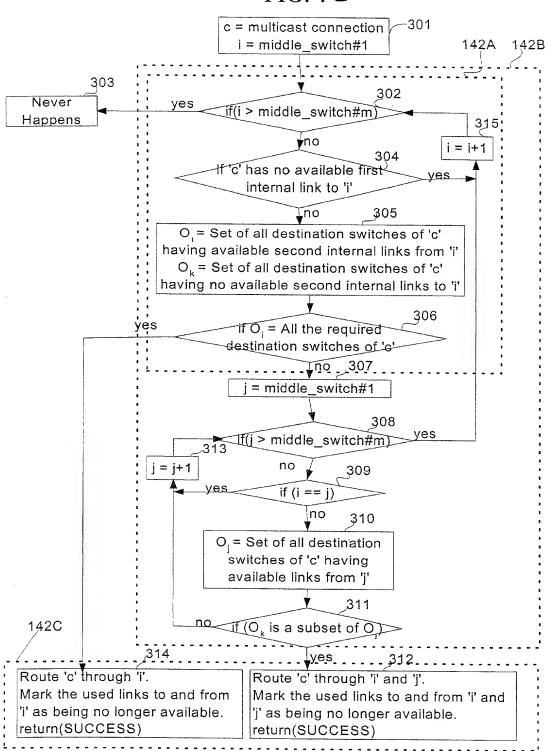


FIG. 4D 580 500 Controller Memory Availability status of all output switches 081 570-1 Α OS2 U 510 OS3 Α Middle Connection c : į switches OSr U MS1 Destination List of c MS2 OSi MS3 OS1 560 570-2 OS2 OSj MSm OS3 A 1 į OSk OSr 520 1 **OS1** OSr Α OS2 U 570-m OS3 Α List of unavailable List of available destinations of c destinations of c through MSi OSr U through MSi OSi OSi OSi OSi 540 OSk OSk 530 OSr OSr List of available destinations of c through MSj OSi OSj **550** OSk 1

OSr